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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,799	08/19/2002	Weng-Hsing Huang	9222-US-PA	4097

31561 7590 11/18/2002

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
CIESLEWICZ, ANETA B	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,799	HUANG ET AL.	
	Examiner	Art Unit	
	Aneta B. Cieslewicz	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3, 5 and 6-17 are rejected under 35 U.S.C. 102(b) as being aniticpated by Tsutsumi, US Patent 6,087,727.

Re claim 1, Tsutsumi discloses a memory device, comprising substrate (1); gate oxide layer (7), disposed on a surface of the substrate; gate (11), disposed on a portion of the gate oxide layer; buried drain line (12a,b), located in the substrate beside both sides of the gate; spacer (15), disposed on sidewalls of the gate; deep doped region (16a,b), located in the substrate below a part of the buried drain line, wherein the buried drain line and the deep doped region together form a bit line of the memory device; an insulation layer (19), disposed above the bit line; and a word line (20), disposed above the gate and the insulation layer, perpendicular to a direction of the bit line.

Re claim 2, in the memory device disclosed by Tsutsumi the insulation layer is formed from silicon oxide (i.e. column 10, line 22).

Re claim 3, in the memory device disclosed by Tsutsumi the spacer (15) is formed from silicon oxide (i.e. column 9, line 59).

Re claim 5, in the memory device disclosed by Tsutsumi the deep-doped region (16a,b) is located in the substrate beside both sides of the spacer (i.e. column 9, line 64).

Re claim 6, Tsutsumi discloses a fabrication method for a memory device, comprising: forming a gate oxide layer (7) on a substrate (1); forming a bar-shaped conductive structure (11) on the gate oxide layer, wherein a cap layer (9) is formed on a top of the bar-shaped conductive structure; forming a buried drain line (12a,b) in the substrate beside both sides of the bar-shaped conductive structure; forming a spacer (15) on sidewalls of the bar-shaped conductive structure and the cap layer; forming a deep doped region (16a,b) in the substrate beside both sides of the spacer, wherein the buried drain line and the deep doped region together form a bit line of the memory device; forming an insulation layer (19) above the bit line; removing the cap layer; forming a conductive layer on the substrate; and patterning the conductive layer and the bar-shaped conductive structure in a direction perpendicular to a direction of the bit line to form a word line and a plurality of gates.

Re claim 7, in the method disclosed by Tsutsumi, there is an etching selectivity between the cap layer (36) and the spacer (15).

Re claim 8, in the method disclosed by Tsutsumi, there is an etching selectivity between the cap layer (36) and the insulation layer (19).

Re claim 9, in the method disclosed by Tsutsumi the cap layer is formed with a material comprising silicon nitride (i.e. column 18, line 3).

Re claim 10, in the method disclosed by Tsutsumi, the spacer is formed with a material comprising silicon oxide (i.e. column 9, line 59).

Re claim 11, in the method of disclosed by Tsutsumi insulation layer is formed with a material comprising silicon oxide (i.e. column 10, line 22).

Re claim 12, in the method of disclosed by Tsutsumi, forming of the buried drain line (12a,b) includes performing an ion implantation process using the cap layer and the bar-shaped conductive structure as an implantation mask (i.e. column 9, line 58).

Re claim 13, in the method disclosed by Tsutsumi, the deep-doped region (16a,b) is formed by performing an ion implantation process using the cap layer and the spacer as an implantation mask (i.e. column 9, line 64).

Re claim 14, in the method disclosed by Tsutsumi, forming of the insulation layer above the bit line comprises: forming globally an insulation material on the substrate, the insulation layer covers the cap layer; and removing a portion of the insulation material until the cap layer is exposed (i.e. column 10, lines19-26).

Re claim 15, in the method disclosed by Tsutsumi, removing the portion of the insulation material includes performing back etching or chemical mechanical polishing (i.e. column 10, lines 19-26).

Re claim 16, in the method disclosed by Tsutsumi, forming of the bar-shaped conductive structure and the cap layer comprises: forming sequentially a conductive layer and a material (cap) layer on the gate oxide layer; and patterning the material layer and the conductive layer to form the bar-shaped conductive structure and the cap layer (i.e. column 9, lines 40-51).

Re claim 17, in the method disclosed by Tsutsumi, forming the spacer comprises: forming a conformal silicon layer on the substrate and back-etching the conformal silicon oxide layer to form the spacer (i.e. column 9, line 59-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsumi, US Patent 6,087,727.

Re claim 4, the memory device disclosed by Tsutsumi includes all the limitations claimed except that the word line is formed from polysilicon. Tsutsumi, however, discloses polysilicon, metal silicides, metal nitrides, Al and Cu as alternative conductive materials (i.e. column 14, lines 29-31). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the word line in the device of Tsutsumi from polysilicon in order to obtain a high quality interface between the word line and the polysilicon gate and silicon oxide insulation layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aneta B. Cieslewicz whose telephone number is (703) 308-7607. The examiner can normally be reached M-F (8:00 a.m. - 4:30 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached at (703) 308-4918. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

ABC
November 8, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800